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Partner Search Form

INSTITUTION/CONTACT PERSON:			
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INFORMATION ABOUT THE PLANNED PROJECT:		
Erasmus+ International co-operation Activity (higher education sector) – **type of the project idea**	**Please, tick the appropriate one/ones:** ☑ **Erasmus+ KA1: International students and staff credit mobility** ☐ **Erasmus+ KA1: Erasmus Mundus Joint Master Degrees** ☐ **Erasmus+ KA2: Capacity Building Higher Education in Partner Countries** ☐ **Erasmus+ Jean Monnet programme**	
Discipline / Academic field	**Electrical Engineering/Nanotechnology**	
Institution's preferable role in the project?(applicant/partner)	☐ **Applicant** ☑ **Partner**	
Which countries are about to be involved?	**Erasmus+ Programme Countries**	**Germany, France, Spain, Italy**
	Erasmus+ Partner Countries	
Working language of the project consortium = language of the project application	**English**	
Duration of the project	**2 Months**	

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PROJECT DESCRIPTION:

Objectives:

Current circuit and device designs are based on worst scenarios resulting in significant waste of wafer real estate. This is due to lack of physic-based statistical models that accurately predict the gate dielectric defect levels, the fraction of these defects that are active during device operation, the variation of the number, position and characteristics of these dielectric traps at time-zero and as a function of operation time, as well as the effect of this variation on the device parameters.

Activities

Current statistical models are not based on experimental results, and do not consider the correlation between charge carrier number and mobility fluctuations. In addition, so far the researchers have focused either on time-zero variability of trapping/detrapping or time-dependent variability of the same phenomenon with no attention to correlation between the two. Spatial distribution of the traps has been limited, in the existing models, to the silicon/dielectric interface with no regard to the trap distribution into the oxide.

The work will start with experimental investigation of random telegraph signals on MOSFET or FinFET samples to investigate the defect properties in the gate-dielectric oxide. The electrical activity of these defects that transform them into charge carrier traps – activation energy, capture cross-section, screened scattering coefficient, capture and emission times – will be characterized. All these characteristics will be investigated under variable temperatures using passive cryogenic system.

Results

The effect of electrical stressing like hot-carrier stressing and shallow trench isolation induced stress, respectively, will be experimentally investigated. Their effect on the charge carrier trapping by the dielectric defects will be investigated as a function of time. The models built during the previous phase will be fine-tuned to predict the increased variability due to these stress conditions. After we developed the statistical model, it will be fed into a simulation which is going to be developed in house.

We are searching for:

Types of institutions	R1- Schools which are dealing with nanotechnology and device physics.
Country/Region	Germany, Spain, France, England, Italy.
Institutions' profiles	

Other relevant information	